

Notice of References Cited	Application/Control No. 10/734,905	Applicant(s)/Patent Under Reexamination HWANG ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,537,341	07-1996	Rose et al.	716/16
	B	US-6,150,838	11-2000	Wittig et al.	326/39
	C	US-6,557,144 B1	04-2003	Lu et al.	716/2
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Cong et al., "On Area/Depth Trade-Off in LUT-Based FPGA Technology Mapping", June 1994, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 2, iss. 2, pp. 137 - 148.
	V	Cong et al., "Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-Based FPGA Design", June 1996, IEEE Design Automation Conference Proceedings, pp. 726 - 729.
	W	Habib et al., "Technology Mapping Algorithms for Sequential Circuits Using Look-up Table Based FPGAS", Mar. 1995, IEEE Fifth Great Lakes Symposium, VLSI Proceedings, pp. 164 - 167.
	X	Rawski et al., "Non-Disjoint Decomposition of Boolean Functions and Its Application in FPGA-oriented Technology Mapping", Sept. 1997, IEEE Proceedings of the 23rd EUROMICRO Conference on New Frontiers of Information Technology, pp. 24 - 30.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	K	US-			
	L	US-			
	M	US-			

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Martin et al., "A Comparing Study of Technology Mapping for FPGA", Feb. 1998, IEEE Proceedings, Design, Automation and Test in Europe, pp. 939 - 940.
	V	Lu et al., "Technology Mapping for Simultaneous Gate and Interconnect Optimization", Jan. 1999, IEEE Proceedings on Computers and Digital Techniques, vol. 146, iss. 1, pp. 21 - 31.
	W	Cong et al., "Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-Based FPGA Designs, Apr. 2000, IACM Transactions on Design Automation of Electronic Systems, vol. 5, No. 2, pp. 193 - 225.
	X	Legl et al., "A Boolean Approach to Performance-Directed Technology Mappings for LUT-Based FPGA Design", June 1996, IEEE Design Automation Conference Proceedings, pp. 730 - 733.

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lin et al., "Feasibility of Fixed-Point Transversal Adaptive Filters in FPGA Devices with Embedded DSP Blocks", July 2003, Proceedings, The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications, pp. 157 - 160.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.